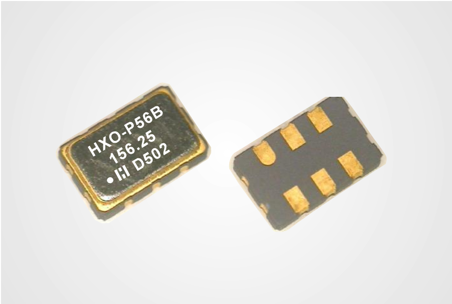
• D5SP Series 5.0*3.2 LV_ PECL OSC



FEATURES

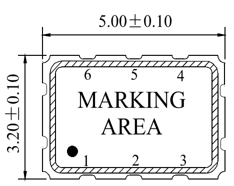
- 5.0*3.2*1.3mm package
- Tri-State function available
- Low Jitter and Noise
- PECL output
- Ideal for Fiber-optic communication applications, FTTH and SONET/SDH applications, Sever, FCHBA, Fibre Channel, Gigabit Ethernet, and Serial ATA

Electrical Specifications

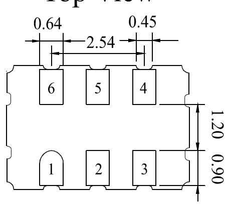
Parameter		Condition	D5SP	
Frequency Range	F0		25~156.25MHz	
Output Specification			LV-PECL	
Frequency Stability*		All Condition	±25ppm, ±50ppm, ±100ppm	
Operating Temperature Range	T_{OPR}		-20℃~+70℃(-40℃~+85℃ option)	
Storage Temperature Range	T_{STG}		-55℃~+125℃	
Power supply Voltage	V_{DD}		3.3V+/-5%	2.5V+/-5%
Supply Current	I_{DD}		90mA Max	
Output Symmetry	Sym	At ½Vpp	40/60%(45/55% Option)	
Rise time	T_r	20%Vpp~80%Vpp	1nS Max	
Fall Time	T_f	80%Vpp~20%Vpp	1nS Max	
Output Voltage	V_{OH}		V_{DD}-1.025V Min.	
	V_{OL}		V_{DD}-1.62V Max.	
Output Load			50 Ω to V_{DD}-2.0V	
Integrated phase jitter (RMS)		Integrated 12KHz to 20MHz	1pS Max	
Start Time	Ts		10mS Max	
Aging(First Year)		25℃±3℃	±2ppm Max	
Pin 1,tri-state function			Pin 1=H or open....Output active at pin 4,5	
			Pin 1=L.....high impedance at pin 4,5	
Packing Unit			1000pcs/reel	

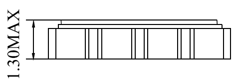
**Include: 25℃ tolerance, operating temperature range, input voltage change, aging, load change, shock and vibration*

Mechanical Dimensions(mm)



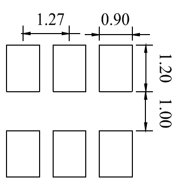
Top View



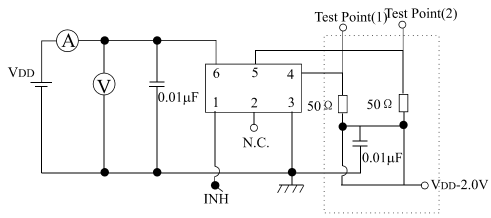


Pin	Connection
#1	Tri-State
#2	N.C.
#3	GND
#4	Comp. Output
#5	Out
#6	V_{DD}

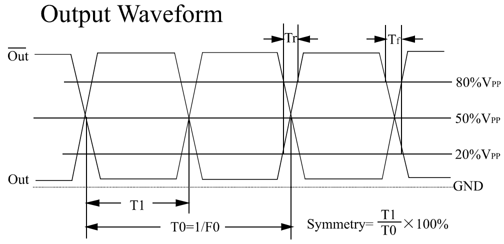
Recommended Solder Pattern



Test Circuit



Output Waveform



**Note: 0.01uF bypass capacitor should be placed between V_{DD}(Pin6) and GND(Pin3) to Minimize power supply line noise